REMARKS

In the Official Action, all pending claims 1-19 were rejected by the Examiner. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

First Rejection under 35 U.S.C. § 103

The Examiner rejected claims 1, 6, 12 and 16 under 35 U.S.C. § 103 (a) as being unpatentable over Poisner et al. (U.S. Patent No. 5,802,269) in view of Nunez et al. (U.S. Patent No. 6,272,601). Specifically, with regard to independent claims 1 and 12, the Examiner stated:

> In reference to Claim 1, Poisner teaches a system comprising: a processor (See Figure 2 Number 31); a main memory operably coupled to the processor (See Figure 2 Number 35); a cache memory operably coupled to the processor (See Figure 2 Number 39); and a bridge, which is equivalent to a host controller, coupled between the processor and the main memory (See Figure 2 Number 33); the host controller comprising: a memory controller operably coupled to the main memory (See Column 3 Lines 61-63); a processor controller operably coupled to the processor (See Column 3 Lines 64-67); and a coherency controller operably coupled to the cache memory (See Column3 Lines 61-63). Poisner further teaches that the bridge facilitates communications between the processor, the main memory, and the cache memory (See Column 3 Lines 59-67), and thus inherently includes an internal bus structure configured to couple each of the memory controller, the processor controller, and the coherency controller to each other. Poisner does not teach wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type. Nunez teaches the use of an interconnect comprised of buses that are unidirectional and that carry only one type of signal, namely, address or data (See Column 8 Lines 1-2).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez, resulting in the invention of Claim 1, in order to improve performance by eliminating the need for buffers and

> tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez).
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> ...
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> In reference to Claim 12, Poisner teaches a bridge containing first and second controllers that communicate with each other and thus inherently has an internal bus structure comprising a plurality of individual buses (See Column 3 Lines 59-67). Poisner does not teach that the individual buses comprise a unidirectional bus configured to transmit only one signal type. Nunez teaches the use of an interconnect comprised of buses that are unidirectional and that carry only one type of signal, namely, address or data (See Column 8 Lines 1-2).
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> It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez, resulting in the invention of Claim12, in order to improve performance by elimination the need for buffers and tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez).
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> Official Action, pages 2-4.

Applicants respectfully traverse the rejections and assert that the Poisner and Nunez references, taken alone or in combination, fail to render the claimed subject matter obvious. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Additionally, if the Examiner relies on a theory of inherency, the extrinsic evidence must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *See In re Robertson,* 169 F.3d 743, 49 U.S.P.Q.2d 1949 (Fed. Cir. 1999). The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. *See id.* In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or sound and supportable technical reasoning to support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art. *See Ex parte Levy,* 17 U.S.P.Q.2d 1461, 1464 (B.P.A.I. 1990). The Examiner, in presenting the inherency argument, bears the evidentiary burden and must adequately satisfy this burden. *See id.* Regarding functional limitations, the Examiner must evaluate and consider the functional limitation, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. *See* M.P.E.P. § 2173.05(g); *In re Swinehart,* 169 U.S.P.Q. 226, 229 (C.C.P.A. 1971); *In re Schreiber,* 44 U.S.P.Q.2d 1429, 1432 (Fed. Cir. 1997). If the Examiner believes the functional limitation to be inherent in the cited reference, then the Examiner "must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Ex parte Skinner,* 2 U.S.P.Q.2d 1788, 1789 (B.P.A.I. 1986).

The Poisner reference is directed to a method and apparatus for managing peripheral devices coupled to a bus, which may relate to managing power consumption of the peripheral devices in a distributed direct memory access (DDMA) environment. *See* Poisner, col. 1, lines 7-10. In a DDMA environment, which is an enhanced version of the direct memory access (DMA) environment, DMA controllers utilize "handshaking" signals for

communication on the buses. *See id.* at col. 1, lines 52-55. Accordingly, because the DDMA environment is a distributed environment, bus master controllers communicate between various peripheral devices. *See id.* at col. 2, lines 7-16. The Poisner reference discloses a system that includes a bridge 33 coupled to a cache 39, a central processing unit (CPU) 31, and a main memory 35, which operates in a DDMA environment. *See id.* at Fig. 1; col. 3, lines 59-67. As such, the Poisner reference discloses a bus system architecture that provides lower power consumption, which allows a device managing peripheral devices to determine causes for master abort errors.

The Nunez reference relates to memory subsystem micro architectures in a multi-processor system. *See* Nunez , col. 1, lines 21-25. The Nunez reference discloses a multiprocessor architecture that requires a complex protocol for requesting and granting the system bus, which hampers the ability to pipeline process operations that require the use of a local bus. *See id.* at col. 1, lines 34-43. As such, the Nunez reference utilizes unidirectional address and data buses between the set of processors and a memory subsystem driven by a single arbitrator and a unified pipeline through which all memory subsystems operations are passed. *See id.* at col. 1, lines 54-58. This provides a simplified architecture that enables a high degree of subsystem operation pipelining to improve system performance. *See id.* at col. 1, lines 61-63.

In the rejection, the Examiner asserted that the Poisner reference teaches all of the subject matter recited in independent claims 1 and 12, inherently and explicitly, except that the Poisner reference does not teach wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type. Specifically, the Examiner asserted that the bridge 33 is equivalent to the "host controller" recited in the present claims.

Further, the Examiner asserted that Poisner inherently includes an internal bus structure configured to couple each of the memory controller, processor controller, and the coherency controller to each other. In an attempt to cure these deficiencies, the Examiner relied upon the Nunez reference.

However, despite the Examiner's forgoing assertions, the cited references fail to render obvious the claims for at least two reasons. First, the Poisner reference fails to inherently disclose "an internal bus structure configured to couple each of the memory controller , the processor controller and the coherency controller to each other, the internal bus structure comprising a plurality of individual buses," as recited in independent claim 1, or an "internal bus structure comprising a plurality of individual buses," as recited in independent claim 12. Secondly, even if the forgoing assertions were correct, the references fail to disclose "wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type," as recited in claim 1, and "each of the individual buses comprising a unidirectional bus configured to transmit only one signal type," as recited in claim 12. Hence, Applicants respectfully submit that the Poisner and Nunez references fail to disclose all the subject matter recited in independent claims 1 and 12, as discussed below.

With regard to the first point, the Poisner and Nunez references fail to disclose "an internal bus structure configured to couple each of the memory controller, the processor controller and the coherency controller to each other, *the internal bus structure comprising a plurality of individual buses*," as recited in independent claim 1, and an "internal bus structure *comprising a plurality of individual buses*," as recited in independent claim 12. (Emphasis added). In the rejection, the Examiner only asserted that the Poisner reference inherently teaches and inherently includes an internal bus structure configured to couple each of the

memory controller, process controller and the coherency controller to each other. The Examiner did not even assert that Poisner discloses an internal bus structure "comprising a plurality of individual buses," as recited in claims 1 and 12. Regardless, the Examiner's unsupported assertion does not provide a basis in fact and/or sound reasoning to support the determination that the allegedly inherent characteristic *necessarily flows* from the teachings of the Poisner reference. Therefore, the Examiner has not satisfied the evidentiary burden required by the binding precedence's cited above. Indeed, the Poisner reference cannot support the Examiner's burden. The Poisner reference does not disclose or describe any interconnectivity within the first bridge circuit 33, which is alleged to be equivalent to the "host controller" of the present claims. Nothing in the Poisner reference suggest the necessity of an internal bus structure configured to couple the memory controller, process controller and the currency controller to each other. Accordingly, the "an internal bus structure configured to couple each of the memory controller, the processor controller and the coherency controller to each other, the internal bus structure comprising a plurality of individual buses," as recited in independent claim 1, and the "internal bus structure comprising a plurality of individual buses," as recited in independent claim 12, is not inherently found in the Poisner reference.

Further, the Nunez reference does not cure the deficiencies of the Poisner reference. The Nunez reference discloses a computer system 100 comprises a memory subsystem 108 along with a set of processors 104a-104n. *See* Nunez, Fig. 1; col. 7, lines 30-35. The processors 104a-104n are connected to the memory subsystem 108 via local interconnects 106. *See id.* at col.7, lines 49-67. Clearly, no host controller, much less, a processor controller is shown in the Nunez reference. As such, the Nunez reference does not even disclose a host controller, much less, a host controller having a memory controller, a process

controller, a coherency controller or any internal bus structure for coupling such controllers, wherein the internal bus structure comprises a plurality of individual buses. Accordingly, because the Nunez reference does not disclose the claimed subject matter, it fails to cure the deficiencies of the Poisner reference.

With regard to the second point, the Poisner and Nunez references fail to disclose "wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type," as recited in claim 1, and "each of the individual buses comprising a unidirectional bus configured to transmit only one signal type," as recited in claim12. In the rejection, the Examiner admitted that the Poisner reference does not teach this recited feature. In an attempt to cure this deficiency, the Examiner relied upon the Nunez reference to teach the claimed subject matter.

Contrary to the Examiner's assertion, the Nunez reference does not teach an internal bus structure comprising individual buses each having a unidirectional bus configured to transmit only one signal type. In the rejection, the Examiner relied upon a specific passage of the Nunez reference, at column 8, lines 1-4, to provide support for the recited feature. This passage simply describes that an interconnect 106 may include unidirectional data and address buses that improve performance by eliminating the need for buffers and tri-state drivers associated with bi-directional buses. *See id.* At best, the Nunez reference discloses unidirectional data and address buses. This is in contrast to the present claims, which recite using individual buses configured to transmit only one signal type. The signal type in the present application is associated with each of the individual signals associated with a transaction. One of the advantages of the recited subject matter is that the internal bus structure provides point-to-point connections of the individual buses 30A-30K, each carrying

an individual and unique signal associated with a particular transaction. *See* Application, page 12, lines 13-14. For example, in the present application, the signal types are described to include a request address/command signal, and an initial response signal, a request snoop results signal, a snoop address/command signal, etc. *See id.* at Fig. 3; page 17, line 14, page 19, line 8. As such, the Nunez reference does not disclose multiple unidirectional buses, each configured to transmit only one signal type under any reasonable interpretation of the claim terms. Accordingly, because the Nunez reference does not disclose the claimed subject matter, it fails to cure the deficiencies of the Poisner reference.

Because the Nunez and Poisner references fail to disclose all of the cited features in the instant claims, the cited references cannot possibly render the claimed subject matter obvious. Therefore, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1, 6, 12, and 16.

Second Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 2-5 and 13-15 under 35 U.S.C. § 103(a) as being unpatentable over Poisner et al. (U.S. Patent No. 5,802,269) in view of Nunez et al. (U.S. Patent No. 6,272,601) and Kosaraju (U.S. Patent Application Publication No. 2002/0073261). Applicants respectfully traverse the rejection.

Claims 2-5 depend from independent claim 1 and claims 13-15 depend from independent claim 12. Accordingly, claims 2-5 and 13-15 are believed to be patentable based on this dependency, as well as the subject matter recited in each of the respective claims. In the rejection, the Examiner relied upon the Kosaraju reference to teach connecting devices together using a point-to-point bus, wherein each device is connected to only one other

device. However, contrary to the Examiner's assertion, the Kosaraju reference teaches a fully meshed point-to-point architecture between four processors 504, 506, 508, 510 and an input-output component 502. *See* Kosaraju, page 2, paragraph 24. In the reference, each of the four processors 504, 506, 508, 510 utilize an arbiter that enables a customer to change the number of ports linked between a processor and devices external to the processor. *See id.* at page 2, paragraph 19. Clearly, the Kosaraju reference does not disclose the specific connectivity between the memory controller, process controller, and coherency controller in the claim recitations. As such, the Kosaraju reference fails to disclose the claimed subject matter of claims 2-5 and 13-15. Therefore, because the Kosaraju reference fails does not cure the deficiencies of the Poisner and Nunez references, and does not disclose the claimed subject matter, claims 2-5 and 13-15 are patentable by virtue of their dependency on the respective independent claims 1 and 12, as well as by virtue of the subject matter specifically recited in each claim. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of the claims 2-5 and 13-15.

Third Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 7, 8, 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Poisner et al. (U.S. Patent No. 5,802,269) in view of Nunez et al. (U.S. Patent No. 6,272,601) and Hanaoka et al. (U.S. patent No. 6,584,103). Applicants respectfully traverse this rejection.

Claims 7 and 8 depend from independent claim 1 and claims 17 and 18 depend from independent claim 12. Based on these dependencies, claims 7, 8, 17 and 18 are believed to be patentable over the cited combination. In the rejection, the Examiner admitted that the Poisner and Nunez references failed to teach that each respective signal type includes an

identification tag. In attempt to remedy this deficiency, the Examiner relied upon the Hanaoka reference to disclose the recited features of claims 7, 8, 17 and 18. However, the Hanaoka reference simply describes an effective communication apparatus for transmitting and receiving packets with a label for distinguishing each packet. *See* Hanaoka reference, col. 4, lines 6-12. The Hanaoka reference further illustrates a packet constructed in accordance with IEEE 1394 interface that includes a packet header, destination ID, source ID, transaction label and transaction code within the packet. *See* Hanaoka, Fig. 4, col. 2, lines 49-59. The reference does not disclose or suggest the internal bus structure comprising a plurality of individual buses, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type, as discussed above. As such, the Hanaoka reference does not cure the deficiencies of the Nunez and Poisner references. Therefore, claims 7, 8, 17 and 18 are patentable by virtue of their dependency on the respective independent claims. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claims 7, 8, 17 and 18.

Fourth Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 9 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Poisner et al. (U.S. Patent No. 5,802,269) in view of Nunez et al. (U.S. Patent No. 6,272,601), Hanaoka et al. (U.S. patent No. 6,584,103), and Ketseoglou et al. (U.S. Patent No. 6,130,886). Applicants respectfully traverse this rejection.

Claim 9 depends from independent claim 1 and claim 19 depends from independent claim 12. Based on this dependency, as well as the subject matter recited in each claim, claims 9 and 19 are believed to be patentable over the cited references. In the rejection, the Examiner admitted that the Poisner, Nunez and Hanaoka references do not teach that the

cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete. In an attempt to cure this deficiency, the Examiner relied upon the Ketseoglou reference to disclose this feature. However, the Ketseoglou reference simply describes an integrated communication system, which communicates with multiple communication protocols. *See* Ketseoglou, col. 3, lines 11-21. In the reference, a poll message 402 may include a correlative ID that is a temporary shorthand identifier specific to the user station 102. *See id.* at col. 11, lines 58-65. The correlative ID, which is located in a correlative ID field 722, is used to temporarily identify one or more channels as being allocated to a specific user station 102. *See id.* at col. 13, lines 53-61. The correlative IDs are assigned for the duration of a call connection and reused after termination of the connection. *See id.* Clearly, the reference does not disclose that it may be freed for reuse before the transaction in a request operation is complete. Specifically, the Ketseoglou reference does not disclose "wherein the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete," as recited in claim 9, and "wherein the cycle identification includes a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete," as recited in claim 19. Therefore, because the Ketseoglou reference does not cure the deficiencies of the Poisner, Nunez, and Hanaoka references nor disclose the additionally claimed subject matter, claims 9 and 19 are patentable by virtue of their dependency on the respective independent claims, as well as by virtue of the subject matter specifically recited in each claim. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claims 9 and 19.

Fifth Rejection Under 35 U.S.C. § 103

In this rejection under 35 U.S.C. § 103, the Examiner rejected claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Poisner et al. (U.S. Patent No. 5,802,269) in view of Nunez et al. (U.S. Patent No. 6,272,601) and Miyao et al. (U.S. Patent No. 5,901,281). Applicants respectfully traverse this rejection.

Claim 10 depends from independent claim 1 and is believed to be patentable based upon this dependency. In the rejection, the Examiner admitted that the Poisner and Nunez references do not teach that a processor comprises a cache memory. In an attempt to remedy this deficiency, the Examiner relied upon the Miyao reference to disclose this feature. The Miyao reference is directed to providing redundancy for a cache memory and a clock on a board. *See* Miyao, col. 3, lines 64; or col. 4, line 15. The Miyao reference does not disclose or suggest the processor controller, the internal bus structure comprising a plurality of individual buses, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type, as recited in claim 1. As such, the Miyao reference does not cure the deficiencies of the Poisner and Nunez references, as discussed above. Therefore, claim 10 is patentable by virtue of its dependency on independent claim 1. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claim 10.

Sixth Rejection Under 35 U.S.C. § 103

The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Poisner et al. (U.S. Patent No. 5,802,269) in view of Nunez et al. (U.S. Patent No. 6,272,601) and Deshpande et al. (U.S. patent No. 6,587,930). Applicants respectfully traverse this rejection.

Claim 11 depends from independent claim 1 and is believed to be patentable based upon this dependency. In the rejection, the Examiner admitted that the Poisner and Nunez references do not teach a plurality of processor buses; a plurality of processing units; wherein each processing unit is coupled to a respective one of the plurality of processor buses; and a plurality of processor controllers, each processor controller corresponding to a respective one of the plurality of processor buses, wherein the processor controllers are not directly coupled to each other via the internal bus structure. In an attempt to remedy this deficiency, the Examiner relied upon the Deshpande reference to disclose this feature. However, the Deshpande reference describes a controller that provides coherency by blocking certain commands from a master device. *See* Deshpande, col. 2, lines 24-33. As such, the Deshpande reference simply describes a multiprocessor system coupled through a system bus. *See* Deshpande, Figs. 3-4; col. 4, lines 53-66. The reference does not disclose or suggest the processor controller, the internal bus structure comprising a plurality of individual buses, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type. As such, the Deshpande reference does not cure the deficiencies of the Poisner and Nunez references, which are discussed above. Therefore, claim 11 is patentable virtue of its dependency upon independent claim 1. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claim 11.

Conclusion

In view of the remarks set forth above, Applicants respectfully request reconsideration of the Examiner's rejections and allowance of all pending claims 1-19. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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